PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference P205-0062WO	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/JP2005/005297	International filing date *(day/month/year)* 16 March 2005 (16.03.2005)	Priority date *(day/month/year)* 17 March 2004 (17.03.2004)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant CANON KABUSHIKI KAISHA		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 14 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☒	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 08 December 2006 (08.12.2006)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Authorized officer Masashi Honda e-mail: pt08@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)* see form PCT/ISA/210 (second sheet)	
Applicant's or agent's file reference see form PCT/ISA/220	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/JP2005/005297	16.03.2005	17.03.2004

International Patent Classification (IPC) or both national classification and IPC
INV. G06N3/04

Applicant
CANON KABUSHIKI KAISHA

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☒ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office - P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Tx: 31 651 epo nl Fax: +31 70 340 - 3016	see form PCT/ISA/210	Schenkels, Paul Telephone No. +31 70 340-2639

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/JP2005/005297

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material:

      ☐ on paper

      ☐ in electronic form

   c. time of filing/furnishing:

      ☐ contained in the international application as filed.

      ☐ filed together with the international application in electronic form.

      ☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

Box No. IV Lack of unity of invention

1. ☒ In response to the invitation (Form PCT/ISA/206) to pay additional fees, the applicant has, within the applicable time limit:

   ☒ paid additional fees

   ☐ paid additional fees under protest and, where applicable, the protest fee

   ☐ paid additional fees under protest but the applicable protest fee was not paid

   ☐ not paid additional fees

2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose not to invite the applicant to pay additional fees.

3. This Authority considers that the requirement of unity of invention in accordance with Rule 13.1, 13.2 and 13.3 is

   ☐ complied with

   ☒ not complied with for the following reasons:

   see separate sheet

4. Consequently, this report has been established in respect of the following parts of the international application:

   ☒ all parts.

   ☐ the parts relating to claims Nos.

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1 - 7, 9,-11 - 19, 21 - 24
	No:	Claims	8,20
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-24
Industrial applicability (IA)	Yes:	Claims	1-24
	No:	Claims	

2. Citations and explanations

   see separate sheet

Re Item IV.

This Authority considers that there are 2 inventions covered by claims 1 - 24 indicated as follows:

I: Claims 1 - 9, 11 - 21, 23, and 24 directed to a parallel pulse processing apparatus and method using a gate circuit to neglect parts of the data
II: Claims 10 and 22 directed to a parallel pulse processing apparatus and method storing and reusing intermediate data in memories

The reasons for which the inventions are not so linked as to form a single general **inventive** concept, as required by Rule 13.1 PCT, are as follows:

1. The prior art document US5263122 discloses a pulse processing apparatus including input and output means and a plurality of arithmetic elements (a spiking neural network, depicted in figure 1).
   The potential special technical feature of subject 1, as defined by Rule 13.2 PCT and not known from the prior art as disclosed by the document US5263122, can be found in claim 1 and must be seen as the presence of a gate circuit within the apparatus capable of routing or neglecting the signals according to their signal level.
   The underlying problem of subject 1, solved by the solution proposed in claim 1, can thus be seen as how to reduce hardware and time constraints by neglecting parts of the data.

2. The potential special technical features of the second subject can be seen as the presence of memories within a pulse processing apparatus for storing intermediate results and input means for inputting the intermediate results.
   From this special technical feature, as disclosed in claim 10, the underlying technical problem can be seen as how to use the hardware more efficiently by reusing pre-processed data.

3. There are thus no same or corresponding special technical features in the claimed inventions within the meaning of Rule 13.2 PCT. It is especially pointed out that the

common feature of the parallel pulse apparatus as technical application of the two above described inventions cannot be regarded as common **inventive** concept as it is clearly disclosed in US5263122.
The application does hence not meet the requirements of Unity of Invention as defined in PCT regulations Rule 13.2, also taking Rule 13.3 into consideration.
The search has been performed, according to PCT regulations Article 17(3)(a) on those parts of the international application which relate to the invention first mentioned in the claims (i.e. claims 1 - 9, 11 - 21, 23 and 24).

Re Item V.

1 Reference is made to the following documents:

D1: EP-A-1 262 912 (CANON KABUSHIKI KAISHA) 4 December 2002 (2002-12-04)
D2: US-A-5 704 016 (SHIGEMATSU ET AL) 30 December 1997 (1997-12-30)
D3: US-A-5 263 122 (NUNALLY ET AL) 16 November 1993 (1993-11-16)

FIRST INVENTION

2 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 1 - 7, 9, 11 - 19, 21, 23 and 24 does not involve an inventive step in the sense of Article 33(3) PCT and claims 8 and 20 are not novel in the sense of Article 33(2) PCT.

2.1 The document D1 is regarded as being the closest prior art to the subject-matter of claim 1, and discloses a parallel pulse signal processing apparatus including a plurality of pulse output arithmetic elements, a plurality of connection elements which

parallelly connect predetermined elements of the arithmetic elements (D1, abstract, figures 3 & 8). It discloses as well a gate circuit which selectively passes pulse signals from the plurality of connection elements (D1, p. 19, l. 38: "For instance, according to a topology in FIG. 11, a so-called Winner-Take-All (WTA) circuit for detecting the maximum output is provided between the feature integration layer neuron group and the phase synchronization circuit").

The apparatus is characterized in that said arithmetic element comprises modulation processing means for executing predetermined modulation processing on the basis of the plurality of time series pulse signals which are input (D1, p. 5, l. 54-57: "In the synaptic circuit S202, a so-called excitatory connection involves amplifying the pulse signals, while an inhibitory connection involves attenuating the signals. In the case of transmitting the information through on the pulse signals, the amplification and the attenuation can be actualized by any one of an amplitude modulation, a pulse width modulation, a phase modulation and a frequency modulation of the pulse signal") and input means for inputting a plurality of time series pulse signals and pulse output means for outputting a pulse signal on the basis of a result of modulation processing (D1, p. 6, l. 12-15: "Each of the neuron elements is extension-modelled based on the so-called integrate-and-fire type neuron, and is the same as this integrate-and-fire type neuron in terms of such a point that the neuron element fires when a result of linearly adding the input signals (a pulse train corresponding to an action potential) spatiotemporally exceeds a threshold value, and outputs the pulse signals").

Said gate circuit selectively passes, of the signals from said plurality of connection elements, a finite number of pulse signals (D1, p. 19, l. 35-37: "Moreover, the phase synchronization circuit can be also structured to receive the inputs only from the neurons performing the maximum outputs among the feature integration layer neurons that should receive the inputs in FIG. 10B").

The subject-matter of claim 1 therefore differs from the teaching of D1 in that the gate circuit of claim 1 is not unconditionally a "Winner Take All" circuit, but a general gate circuit selectively passing a finite number of pulse signals according to their signal level. It is however generally known to the person skilled in the art that the feature "Winner Take All" circuit is a specific kind of gate circuit and can be interchanged with that the latter without encountering technical problems where circumstances make it desirable. The gate circuit claimed in the application does not disclose any technical effect other than those already known from D1.

2.2 The same reasoning applies, mutatis mutandis, to the subject-matter of the corresponding independent claim 18, which discloses the same subject matter as claim 1 rephrased as a method claim and which therefore is also considered not inventive.

2.3 The document D1 is regarded as being the closest prior art to the subject-matter of claim 7, and discloses a parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations (D1, p.5, l. 18-20: "The processing at the same scale level (or with the same resolution level) proceeds through each processing channel, wherein the low-order through high-order features are detected and recognized by hierarchical parallel processing").
It also comprises a plurality of arithmetic elements which receive signals from different layer levels and outputs predetermined pulse signals by a predetermined local receptor field structure (D1, p. 5, l. 27-30: "Each of the feature detection layers (1, 1), (1, 2), ..., (1, N) and the feature integration layers ((2, 1), (2, 2), ..., (2, N)) has a predetermined receptive field structure acquired by learning").
It comprises also a gate circuit element which selectively passes the pulse signals from said plurality of arithmetic elements belonging to a predetermined receptor field in accordance with a signal level of the pulse signal (D1, figure 10A, the feature integration layer having a receptive field structure, as cited above and p. 19, l. 38-41: "For instance, according to a topology shown in FIG. 11, a so-called Winner-Take-All for detecting the maximum output is provided between the feature integration layer neuron group and the phase synchronization circuit").
The subject-matter of claim 1 therefore also only differs from the teaching of D1 in that the gate circuit is not unconditionally a "Winner Take All" circuit, but a general gate circuit selectively passing a finite number of pulse signals according to their signal level. It is however generally known to the person skilled in the art that the feature "Winner Take All" circuit is a specific kind of gate circuit and can be interchanged with that the latter without encountering technical problems where circumstances make it desirable. The gate circuit claimed in the application does not disclose any technical effect other than those already known from D1.

2.4 The same reasoning applies, mutatis mutandis, to the subject-matter of the corresponding independent claim 19, which discloses the same subject matter as

claim 1 rephrased as a method claim and which therefore is also considered not inventive.

2.5 The document D1 is regarded as being the closest prior art to the subject-matter of claim 8, and discloses a parallel pulse signal processing apparatus including input means for inputting data in a predetermined dimension, a plurality of data processing means and output means for outputting a result of a pattern detection (D1, abstract, figures 3, 8 & 12, p. 15, l. 30-51). It discloses as well a gate circuit which selectively passes pulse signals from the plurality of connection elements (D1, p. 19, l. 38: "For instance, according to a topology in FIG. 11, a so-called Winner-Take-All (WTA) circuit for detecting the maximum output is provided between the feature integration layer neuron group and the phase synchronization circuit").
The apparatus is characterized in that said data processing means includes a plurality of arithmetic elements parallelly connected by predetermined connection means (D1, figure 3).
Said arithmetic element included in said data processing means outputs a pulse-shaped signal train representing a detection result of a pattern of a predetermined category on the basis of an arrival time pattern of a plurality of pulses from predetermined arithmetic elements input in a predetermined window (D1, figure 3 and p. 9, l. 43-48: "Next, pulse encoding of a two-dimensional graphic pattern and a detection method thereof will be explained [...] As a result, so far as the pulses are outputted from the neurons of the feature integration layer, pulses of a pulse train Pi are set to arrive at the neuron n'j in a predetermined sequence (such as P4, P3, P2, P1 in FIG. 3A), depending on a delay quantity at the synaptic connection that is determined by learning").
Said output means outputs the detection result of the predetermined pattern in the data on the basis of the outputs from said arithmetic elements (D1, abstract, figures 3, 8 & 12, p. 15, l. 30-51).
Hence all features of claim 8 are known from the prior art and the claim is not considered to be novel.

2.6 The same reasoning applies, mutatis mutandis, to the subject-matter of the corresponding independent claim 20, which discloses the same subject matter as claim 1 rephrased as a method claim and which therefore is also not considered to

be novel.

2.7 The document D1 is regarded as being the closest prior art to the subject-matter of claim 9, and discloses a parallel pulse signal processing apparatus including input means for inputting data in a predetermined dimension, a plurality of data processing means and output means for outputting a result of a pattern detection (D1, abstract, figures 3, 8 & 12, p. 15, l. 30-51).
The apparatus is characterized in that said data processing means includes a plurality of arithmetic elements parallelly connected by predetermined connection means (D1, figure 3).
Said gate circuit selectively passes the pulse signals on the basis of signal levels of the pulse signals from said plurality of data processing means (D1, p. 19, l. 35-37: "Moreover, the phase synchronization circuit can be also structured to receive the inputs only from the neurons performing the maximum outputs among the feature integration layer neurons that should receive the inputs in FIG. 10B").
Said arithmetic elements receive a time series pulse signal, identify time series pulse signal patterns of a plurality of classes, and output a pulse-shaped signal train unique to an arrival time pattern of a plurality of predetermined pulse signals input in a predetermined time window (D1, figure 3 and p. 9, l. 43-48: "Next, pulse encoding of a two-dimensional graphic pattern and a detection method thereof will be explained [...] As a result, so far as the pulses are outputted from the neurons of the feature integration layer, pulses of a pulse train Pi are set to arrive at the neuron n'j in a predetermined sequence (such as P4, P3, P2, P1 in FIG. 3A), depending on a delay quantity at the synaptic connection that is determined by learning").
Said output means outputs the detection result of the predetermined pattern in the data on the basis of the outputs from said arithmetic elements. (D1, abstract, figures 3, 8 & 12, p. 15, l. 30-51).
The subject-matter of claim 9 therefore also only differs from the teaching of D1 in that the gate circuit is not unconditionally a "Winner Take All" circuit, but a general gate circuit selectively passing a finite number of pulse signals according to their signal level. It is however generally known to the person skilled in the art that the feature "Winner Take All" circuit is a specific kind of gate circuit and can be interchanged with that the latter without encountering technical problems where circumstances make it desirable. The gate circuit claimed in the application does not

disclose any technical effect other than those already known from D1.

2.8 The document D1 is regarded as being the closest prior art to the subject-matter of claim 21, and discloses a method of signal processing using a parallel pulse signal processing apparatus comprising input means for inputting data in a predetermined dimension, a plurality of data processing means for outputting pulse signals, a gate circuit which selectively passes signals from the data processing means, and output means for outputting a result of a pattern detection (D1, abstract, figures 3, 8 & 12, p. 15, l. 30-51, claim 1).
The method is characterized by using a gate circuit to selectively pass the pulse signals on the basis of signal levels from the plurality of data processing means (D1, p. 19, l. 35-37: "Moreover, the phase synchronization circuit can be also structured to receive the inputs only from the neurons performing the maximum outputs among the feature integration layer neurons that should receive the inputs in FIG. 10B").
A plurality of arithmetic elements, which are included in the data processing means and parallelly connected by predetermined connection means, is caused to receive a time series pulse signal, identify time series pulse signal patterns of a plurality of classes, and output a pulse-shaped signal train unique to an arrival time pattern of a plurality of predetermined pulse signals input in a predetermined time window (D1, figure 3 and p. 9, l. 43-48: "Next, pulse encoding of a two-dimensional graphic pattern and a detection method thereof will be explained [...] As a result, so far as the pulses are outputted from the neurons of the feature integration layer, pulses of a pulse train Pi are set to arrive at the neuron n'j in a predetermined sequence (such as P4, P3, P2, P1 in FIG. 3A), depending on a delay quantity at the synaptic connection that is determined by learning").
Said output means are caused to output the detection result of the predetermined pattern in the data on the basis of the outputs from said arithmetic elements. (D1, abstract, figures 3, 8 & 12, p. 15, l. 30-51).
The subject-matter of claim 21 therefore also only differs from the teaching of D1 in that the gate circuit is not unconditionally a "Winner Take All" circuit, but a general gate circuit selectively passing a finite number of pulse signals according to their signal level. It is however generally known to the person skilled in the art that the feature "Winner Take All" circuit is a specific kind of gate circuit and can be interchanged with that the latter without encountering technical problems where

circumstances make it desirable. The gate circuit claimed in the application does not disclose any technical effect other than those already known from D1.

2.9 The dependent claims 2 - 6 and 11 - 17 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of inventive step, see document D1, D2 and D3.

SECOND INVENTION

3 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 10 and 22 does not involve an inventive step in the sense of Article 33(3) PCT.

3.1 The document D1 is regarded as being the closest prior art to the subject-matter of claim 10, and discloses

a parallel pulse signal processing apparatus (page 3 , line 21 : parallel pulse signal processing)

which hierarchically executes a plurality of arithmetic processing operations (page 5 , lines 19 - 20 : hierarchical parallel processing),

comprising a plurality of data processing means (page 3 , lines 30 - 31 : comprising a plurality of arithmetic elements),

input means for inputting one of an intermediate result of different layer levels,

having a feature detection layer which detects a plurality of features from the data input by said input means, for outputting pulse signals; said data processing means further comprising a plurality of arithmetic elements which receive detection signals of the features of different types from a layer level of a preceding stage and output predetermined pulse signals (page 5 , lines 21 - 35 . a feature integration layer has a predetermined receptive field structure (the receptive field hereinafter implies a connecting range with an output element of an immediate anterior layer..) and is constructed of neuron elements each generating the pulse train...The latter group of feature integration layers integrate results of detecting the plurality of features from the anterior feature detection layers),

and a gate circuit which selectively passes outputs from said arithmetic elements involved in the plurality of predetermined features, (page 19, lines 38-41: "For instance, according to a topology shown in FIG. 11, a so-called Winner-Take-All for detecting the maximum output is provided between the feature integration layer neuron group and the phase synchronization circuit"). ,

a timing signal generation circuit, wherein said arithmetic elements output pulse-shaped signals at one of a frequency and a timing based on a plurality of input signals from said timing signal generation circuit and an arrival time pattern of a plurality of pulses in a predetermined time window (page 7 , lines 10 - 12 : there may also be utilized such a known circuit architecture as to give forth an oscillatory output delayed by a predetermined timing when the input summation value obtained by use of the window function...).

The subject-matter of claim 1 therefore differs from the teaching of D1 in that input means can additionally input " **data from a predetermined memory** ".

It is not clear what this "data from a predetermined memory" might be nor what problem it solves. The description , although using the expression "data from a predetermined memory" twice as a mere copying of the wording of the claims 10 and 22, also provides no further clarification. As such a meaningful interpretation of the

expression "data from a predetermined memory " is currently not possible.
The mere use of using input data from different sources is commonly known to the man skilled in the art of neural networks (see e.g. D2 : Fig. 1; column 1 , line 64 - column 2 , line 3; column 3 , lines 14 - 16) and therefore is this additional feature not considered as involving an inventive step in the sense of Article 33(3) PCT.

3.2 The same reasoning applies, mutatis mutandis, to the subject-matter of the corresponding independent claim 22, which discloses the same subject matter as claim 10 rephrased as a method claim and which therefore is also considered not inventive.